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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,039	09/30/2003	John K. Walton	EMC2-116AUS	5415

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EXAMINER

ROJAS, MIDYS

ART UNIT PAPER NUMBER

2185

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,039	WALTON ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-6 is/are rejected.
- 7) ☐ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/28/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 10/28/05 has been considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason, JR. et al. (2003/0135674) in view of DeKoning et al. (6,216,199).

Regarding Claim 1, Mason, JR. discloses a system interface (Figures 1 and 2) comprising:

- (a) a plurality of front end directors (the combination of 8, 7 and 10) adapted for coupling to a host computer/server (I/O interface 8 and target interface logic 10 where in an embodiment with multiple hosts, multiple I/O interfaces 8 and 7 would be present, paragraph 56);

(b) a plurality of back end directors (the combination of 2 and 12) adapted for coupling to a bank of disk drives (I/O interface 2 and initiator mode interface logic 12 where in an embodiment with multiple storage devices 3, multiple I/O interfaces 2 would be present, paragraph 55); a data transfer section 13 having cache memory SDRAM, the cache memory being coupled to the plurality of front end and back end directors (SDRAM for cache and control data, paragraph 50);

(c) wherein the front end and back end directors control data transfer between the host computer/server and the bank of disk drives (paragraph 0050), such data passes through the cache memory in the data transfer section as such data passes between the host computer and the bank of disk drives;

Mason, JR. discloses a message network (represented by embedded CPU 11), coupled to the plurality of font end and back end directors (as shown in Figure 2 of Mason, JR., the messages passing are control data that enable the embedded CPU to guide the target interface logic to transmit data to the disk storage unit 3, see paragraph 51). The messages going through the message network by-pass the data transfer section as shown on Figure 2.

Mason, JR. does not teach a cache memory manager.

DeKoning discloses

(d) a cache memory manager interface 124 (Figure 1), adapted to receive queries from the director 102 (receives cache commands from storage processor 102, Col. 4, lines 29-39), such cache memory manager having therein a memory 116 for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives (hash table, Figure 3);

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where in having a memory for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives, the cache memory manager is able to determine whether data to be read from the disk drives or data to be written to the disk drives resides in the cache memory by analyzing its map.

(e) wherein the cache memory manager interface 124 receives the queries from the director 102 and operates independently of the director in processing such queries to search the map stored in the memory thereof to determine for the querying director whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory (Col. 4, lines 29-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Mason, JR. to include a cache memory manager interface as that of DeKoning since the cache memory manager takes control of all cache search and access operations, thus leaving the back end and front end directors to communicate with the disk drives without interruption. In allowing the back end and front end directors to no longer deal with the search of the cache, the resources of the directors are being concentrated in communications with the bank of disk drives, thus allowing them to access the disk drives at a faster rate if the data requested is not present in the cache 220.

Regarding Claim 3, Mason, JR. in view of Dekoning discloses the system wherein the memory 116 in the cache memory manager 124 has a plurality of n locations (hash table 300), each one of the locations corresponding to a location 310 in the disk drives 100, each one of the locations in the memory in the cache memory manager being adapted to store therein a disk

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address and an indication as to whether data stored or to be stored in such disk location is in the cache memory (cache management resource linked list 304, see Col. 8, line 33- Col. 9, line 5).

Regarding Claim 4, Mason, JR. in view of Dekoning discloses the system wherein the logical disk address provided by the host computer/server is hashed (hash table 300) and the memory in the cache memory manager 116 (Figure 3) comprises a plurality of, m , tables, where m is greater than one (hash table 300, linked list 302, resource linked list 304); each one of such m tables has a plurality, n_m locations where the sum of the locations of the m tables equals n (Col. 8, line 33- Col. 9, line 5).

Regarding Claim 5, Mason, JR. in view of Dekoning discloses the system wherein the cache memory manager in response to a query of the memory (search command 602, Figure 6) therein provides an indication as to whether data stored or to be stored in such disk location is in the cache memory (found/not found, 612 and 616), and the hashed logical disk address provided by the host computer/server is fed to address one of the m tables in the cache memory manager (steps 620 and 622).

Regarding Claim 6, Mason, JR. in view of Dekoning discloses the system wherein the system interface includes a message network (represented by embedded CPU 11), such message network operating independently of the data transfer section (independent from Banks of SDRAM 13) and being coupled to the plurality of front end and back end directors (as shown in Figure 2 of Mason, JR.), the front end and back end directors for controlling data transfer between the host computer/server and the bank of disk drives in response to messages passing between the front end directors and the back end directors through the messaging network to facilitate data transfer between host computer/server and the bank of disk drives (the messages

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passing are control data that enable the embedded CPU to guide the target interface logic to transmit data to the disk storage unit 3, see paragraph 51). The messages going through the message network by-pass the data transfer section as shown on Figure 2.

Allowable Subject Matter

5. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Prior Art of Record does not teach nor suggest in the claimed combination a system interface wherein the cache memory manager is disposed in the back end director.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Midys Rojas
Examiner
Art Unit 2185

MR
January 7, 2006


MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
7/9/06